WHAT IS CLAIMED IS:

1. A pad structure of semiconductor device for reducing wire bonding crack, comprising:

a substrate;

an inter-layer dielectric (ILD) layer formed over the substrate;

a first metallic layer formed over the ILD layer;

a second metallic layer formed over the first metallic layer, and a first inter-metal dielectric (IMD) layer formed between the first metallic layer and the second metallic layer, wherein a plurality of first via holes are formed in the first IMD layer; and

a third metallic layer formed over the second metallic layer, and a second inter-metal dielectric (IMD) layer formed between the second metallic layer and the third metallic layer, wherein a plurality of second via holes are formed in the second IMD layer;

wherein the top surfaces of the second via holes compose a special via pattern, and the second IMD layer is divided into a plurality of separated IMD blocks by the second via holes, thereby reducing wire bonding cracks.

2. The pad structure of claim 1, wherein an area proportion between the second via holes and the second IMD layer is larger than that between the first via holes and the first IMD layer.

3. The pad structure of claim 1, wherein the substrate is a silicon substrate.

4. The pad structure of claim 1, wherein the ILD layer is made of borophosphosilicate glass (BPSG).

5. The pad structure of claim 1, wherein a field-oxide layer is further interposed between the substrate and the ILD layer.

6. The pad structure of claim 1, wherein the first IMD layer and the second IMD layer are made of silicon oxide.

7. The pad structure of claim 1, wherein the first via holes and the second via holes are filled with tungsten (W).

8. The pad structure of claim 1, wherein the top surfaces of the second via holes are in a form of chessboard.

9. The pad structure of claim 1, wherein the top surfaces of the second via holes are in a form of concentric frames.

10. The pad structure of claim 1, wherein the top surfaces of the second via holes are in a form of concentric circles.

11. The pad structure of claim 1, wherein the top surfaces of the second via holes are in a form of spider web.

12. A pad structure of semiconductor device for inhibiting wire bonding crack, comprising:

a substrate;

an inter-layer dielectric (ILD) layer formed over the substrate;

a first metallic layer formed over the ILD layer;

a second metallic layer formed over the first metallic layer, and a first inter-metal dielectric (IMD) layer formed between the first metallic layer and the second metallic layer, wherein a plurality of first via holes are formed in the first IMD layer; and

a third metallic layer formed over the second metallic layer, and a second inter-metal dielectric (IMD) layer formed between the second metallic layer and the third metallic layer, wherein a plurality of second via holes are formed in the second IMD layer;

wherein the first IMD layer is divided into a plurality of separated first IMD blocks by the first via holes, and the second IMD layer is divided into a plurality of separated second IMD blocks by the second via holes.

13. The pad structure of claim 12, wherein the second via holes are positioned above and aligned with the first via holes.

14. The pad structure of claim 12, wherein the second via holes are positioned above and staggered from the first via holes.

15. The pad structure of claim 12, wherein top surfaces of the first via holes compose a special first via pattern, and top surfaces of the second via holes compose a special second via pattern.

16. The pad structure of claim 15, wherein the first via pattern is identical with the second via pattern.

17. The pad structure of claim 16, wherein both the first via pattern and the second via pattern are in a form of chessboard.

18. The pad structure of claim 16, wherein both the first via pattern and the second via pattern are in a form of concentric frames.

19. The pad structure of claim 16, wherein both the first via pattern and

the second via pattern are in a form of concentric circles.

20. The pad structure of claim 16, wherein both the first via pattern and the second via pattern are in a form of spider web.

21. The pad structure of claim 12, wherein the substrate is a silicon substrate, and the ILD layer is made of borophosphosilicate glass (BPSG).

22. The pad structure of claim 12, wherein a field-oxide layer is further interposed between the substrate and the ILD layer.

23. The pad structure of claim 12, wherein the first IMD layer and the second IMD layer are made of silicon oxide.

24. The pad structure of claim 12, wherein the first via holes and the second via holes are filled with tungsten (W).

25. A pad structure of semiconductor device for reducing wire bonding crack, comprising:

a substrate;

an inter-layer dielectric (ILD) layer formed over the substrate;

a plurality of metallic layers formed over the ILD layer; and

a plurality of inter-metal dielectric (IMD) layers, wherein each IMD layer is formed between two metallic layers, and has a plurality of via holes;

at least one of IMD layers is divided into a plurality of separated IMD blocks by the via holes formed therein, which the via holes contact one metallic layer closest to a pad bonding layer.

26. The pad structure of claim 25, wherein an area proportion between the via holes and the IMD layer with the separated IMD blocks is larger than that without the separated IMD blocks.

27. The pad structure of claim 25, wherein the ILD layer is made of borophosphosilicate glass (BPSG), and a field-oxide layer is further interposed between the substrate and the ILD layer.

28. The pad structure of claim 25, wherein the IMD layers are made of silicon oxide, and the via holes are filled with tungsten (W).

29. The pad structure of claim 25, wherein the top surfaces of the via holes that separate the IMD layer into the IMD blocks compose a special via pattern.

30. The pad structure of claim 29, wherein the special via pattern is in a form of chessboard.

31. The pad structure of claim 29, wherein the special via pattern is in a form of concentric frames.

32. The pad structure of claim 29, wherein the special via pattern is in a form of concentric circles.

33. The pad structure of claim 29, wherein the special via pattern is in a form of spider web.

34. A pad structure of semiconductor device for inhibiting wire bonding crack, comprising:

a substrate;

an inter-layer dielectric (ILD) layer formed over the substrate;

a plurality of metallic layers formed over the ILD layer; and

a plurality of inter-metal dielectric (IMD) layers, wherein each IMD layer is formed between two metallic layers and has a plurality of via holes;

at least two of IMD layers are divided into a plurality of separated IMD blocks by the via holes formed therein.

35. The pad structure of claim 34, wherein a Nth ($N \geq 2$, N is a positive

integer) IMD layer and a (N−1)th IMD layer are divided into a plurality of separated IMD blocks by a plurality of Nth via holes and (N−1)th via holes, and top surfaces of the Nth via holes and (N-1)th via holes compose a special Nth pattern and a special (N-1) pattern, respectively.

36. The pad structure of claim 35, wherein the Nth via holes are positioned above and aligned with the (N−1)th via holes.

37. The pad structure of claim 35, wherein the n-th via holes are positioned above and staggered from the (N−1)th via holes.

38. The pad structure of claim 35, wherein the Nth via pattern is identical with the (N−1)th via pattern.

39. The pad structure of claim 38, wherein both the Nth via pattern and the (N-1)th via pattern are in a form of chessboard.

40. The pad structure of claim 38, wherein both the Nth via pattern and the (N-1)th via pattern are in a form of concentric frames.

41. The pad structure of claim 38, wherein both the Nth via pattern and the (N-1)th via pattern are in a form of concentric circles.

42. The pad structure of claim 38, wherein both the Nth via pattern and the (N-1)th via pattern are in a form of spider web.

43. The pad structure of claim 34, wherein the ILD layer is made of borophosphosilicate glass (BPSG), and a field-oxide layer is further interposed between the substrate and the ILD layer.

44. The pad structure of claim 34, wherein the IMD layers are made of silicon oxide, and the via holes are filled with tungsten (W).

45. A pad structure of semiconductor device for inhibiting wire bonding crack, comprising:

a substrate;

an inter-layer dielectric (ILD) layer formed over the substrate;

a plurality of metallic layers formed over the ILD layer; and

a plurality of inter-metal dielectric (IMD) layers, wherein each IMD layer is formed between two metallic layers and has a plurality of via holes;

at least two of IMD layers having a plurality of separated IMD blocks, and one of said two IMD layers having the via holes contacting a closest pad

bonding layer.

46. The pad structure of claim 45, wherein a value of (via hole)/(IMD) of the IMD layer with the separated IMD blocks is larger than that of the IMD layer without the separated IMD blocks.

47. The pad structure of claim 45, wherein those separated IMD blocks of at least two IMD layers is aligned with each other.

48. The pad structure of claim 45, wherein those separated IMD blocks of at least two IMD layers is staggered from each other.

49. The pad structure of claim 45, wherein top surfaces of the separated IMD blocks of at least two IMD layers compose a first IMD pattern and a second IMD pattern, respectively.

50. The pad structure of claim 49, wherein the first IMD pattern is identical with the second IMD pattern.

51. The pad structure of claim 50, wherein the first IMD pattern as well as the second IMD pattern comprises a plurality of isolated and rectangular IMD blocks.

52. The pad structure of claim 50, wherein the first IMD pattern as well

as the second IMD pattern comprises a plurality of isolated and concentric IMD frames.

53. The pad structure of claim 50, wherein the first IMD pattern as well as the second IMD pattern comprises a plurality of isolated and concentric IMD circles.

54. The pad structure of claim 50, wherein the first IMD pattern as well as the second IMD pattern comprises a plurality of isolated and honeycombed IMD blocks.

55. The pad structure of claim 45, wherein the ILD layer is made of borophosphosilicate glass (BPSG), and a field-oxide layer is further interposed between the substrate and the ILD layer.

56. The pad structure of claim 45, wherein the IMD layers are made of silicon oxide, and the via holes are filled with tungsten (W).

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